

EAST SEARCH

8/7/2006

| L# | Hits | Search String | Databases |
|-----|-------|--|---|
| S1 | 32571 | (microprocessor\$1 or microcomputer\$1 or computer\$1) with simulat\$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S2 | 1452 | S1 and (performance near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S3 | 382 | S1 and (functional near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S4 | 34 | S1 and (cycle near2 accurate near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S5 | 73 | S2 and S3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S6 | 106 | S4 or S5 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S7 | 2 | S3 and S4 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S8 | 106 | S6 or S7 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S10 | 43 | S8 and (code with (portion\$1 or part\$1 or section\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S11 | 88 | S8 and (simulat\$3 with mode\$1) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S12 | 44 | S8 and ((modif\$4 or chang\$3 or switch\$3) with mode\$1) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S13 | 93 | S8 and ((simulat\$3 with accuracy) or (code with (portion\$1 or part\$1 or section\$1)) or (simulat\$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S14 | 1 | 20030105620 and (simulat\$3 with code with (portion\$1 or part\$1 or section\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S15 | 1 | 20030105620 and (cycle-based same event-based) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S16 | 1 | 6,687662.pn. and ("functional model" same "cycle accurate model") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S17 | 32606 | (microprocessor\$1 or microcomputer\$1 or computer\$1) with simulat\$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S18 | 1454 | S17 and (performance near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S19 | 382 | S17 and (functional near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S22 | 106 | S20 or S21 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S23 | 2 | S19 and S20 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S24 | 106 | S22 or S23 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S25 | 31 | S24 and (simulat\$3 with accuracy) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S26 | 3 | S24 and ((functional near2 (simulat\$3 or model\$1)) with ((delay or execution) near2 time)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S27 | 1 | S17 and ((functional near2 (simulat\$3 or model\$1)) same ((predict\$3 or forecast\$3 or estimat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S28 | 10 | S17 and ((functional near2 (simulat\$3 or model\$1)) with ((delay or execution) near2 time)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S21 | 73 | S18 and S19 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S20 | 34 | S17 and (cycle near2 accurate near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S31 | 38 | S29 and S30 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S32 | 1 | S29 and "VaST Systems Technology" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S30 | 60 | S18 and (accuracy with (portion\$1 or part\$1 or section\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S29 | 492 | S18 and ((code or model) with (portion\$1 or part\$1 or section\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S33 | 38376 | (microprocessor\$1 or microcomputer\$1 or computer\$1) with simulat\$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S34 | 1780 | S33 and (performance near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S35 | 479 | S33 and (functional near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S36 | 47 | S33 and (cycle near2 accurate near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S37 | 92 | S34 and S35 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S38 | 138 | S36 or S37 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |

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| S39 | 5 | S35 and S36 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S40 | 138 | S38 or S39 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S41 | 45511 | (microprocessor\$1 or microcomputer\$1 or computer\$1 or (integrated near2 circuit)) with simulat | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S42 | 4644 | S41 and ((function\$2 or behavior\$2) near2 simulat\$3) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S43 | 6367 | S41 and ((performance or ((delay or cycle or execution or access) near2 tim\$3) or (cycle near2 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S44 | 1730 | S42 and S43 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S45 | 64 | S44 and (accuracy near2 (level or modify\$3 or vary\$3 or alter\$3)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S46 | 400 | S44 and (simulat\$3 with mode) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S47 | 15 | S45 and S46 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S48 | 6176 | S41 and ((performance or ((delay or cycle or access) near2 tim\$3) or (cycle near2 accurate)) wi | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S49 | 160 | S46 and (execut\$3 near2 time) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |
| S50 | 216 | S45 or S47 or S49 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB |

09/888189 Sivaram Krishnan

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Results of search set S24:

| Document | Kind | Codes | Title | Issue Date | Current OR | Abstract |
|----------------|------|-------|--|------------|------------|----------|
| US 20060155411 | A1 | | Model based testing for electronic devices | 20060713 | 700/108 | |
| US 20060150132 | A1 | | Method and system for finding an equivalent circuit representation for one or more elements in a | 20060706 | 716/5 | |
| US 20060122820 | A1 | | Scripting language for domain-specific modification of a simulation model | 20060608 | 703/22 | |
| US 20060122818 | A1 | | Method, system and program product for defining and recording threshold-qualified count events: | 20060608 | 703/17 | |
| US 20060117274 | A1 | | Behavior processor system and method | 20060601 | 716/1 | |
| US 20060089827 | A1 | | Method, system and program product for defining and recording minimum and maximum event co | 20060427 | 703/17 | |
| US 20060089826 | A1 | | Method, system and program product for defining and recording minimum and maximum count | 20060427 | 703/17 | |
| US 20060085176 | A1 | | Generating an optimized system-level simulation | 20060420 | 703/14 | |
| US 20060080076 | A1 | | System-level power estimation using heterogeneous power models | 20060413 | 703/18 | |
| US 20060074725 | A1 | | Method and apparatus for simulating implementation models of business solutions | 20060406 | 705/7 | |
| US 20060069539 | A1 | | Method of generating simulation model | 20060330 | 703/19 | |
| US 20060015862 | A1 | | Reconfigurable measurement system utilizing a programmable hardware element and fixed hard | 20060119 | 717/168 | |
| US 20050273307 | A1 | | TRANSIENT SIMULATION USING ADAPTIVE PIECEWISE CONSTANT MODEL | 20051208 | 703/14 | |
| US 20050273305 | A1 | | Network models of biochemical pathways | 20051208 | 703/11 | |
| US 20050267721 | A1 | | Network models of biological complex systems | 20051201 | 703/11 | |
| US 20050257178 | A1 | | Method and apparatus for designing electronic circuits | 20051117 | 716/2 | |
| US 20050256692 | A1 | | Method of generating a performance model from a functional model | 20051117 | 703/22 | |
| US 20050240895 | A1 | | Method of emulation of lithographic projection tools | 20051027 | 716/19 | |
| US 20050234695 | A1 | | Timing control method of hardware-simulating program and application of the same | 20051020 | 703/19 | |
| US 20050228630 | A1 | | VCD-on-demand system and method | 20051013 | 703/19 | |
| US 20050216248 | A1 | | System and method for block diagram simulation context restoration | 20050929 | 703/22 | |
| US 20050209839 | A1 | | Data processing apparatus simulation | 20050922 | 703/19 | |
| US 20050187747 | A1 | | Method and apparatus for improved simulation of chemical and biochemical reactions | 20050825 | 703/11 | |
| US 20050187746 | A1 | | Method and apparatus for improved modeling of chemical and biochemical reactions | 20050825 | 703/11 | |

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| US 20050187717 A1 | Method and apparatus for integrated modeling, simulation and analysis of chemical and biochemical | 20050825 702/19 |
| US 20050171746 A1 | Network models of complex systems | 20050804 703/2 |
| US 20050156773 A1 | Digital background cancellation of digital to analog converter mismatch noise in analog to digital c | 20050721 341/144 |
| US 20050143968 A9 | RECONFIGURABLE MEASUREMENT SYSTEM UTILIZING A PROGRAMMABLE HARDWARE | 20050630 703/21 |
| US 20050102125 A1 | Inter-chip communication system | 20050512 703/14 |
| US 20050095572 A1 | Methods and systems for providing simulation-based technical training | 20050505 434/362 |
| US 20050071145 A1 | Simulation apparatus, simulation program, and recording medium | 20050331 703/19 |
| US 20050039079 A1 | Test emulator, test module emulator, and record medium storing program therein | 20050217 714/28 |
| US 20040236559 A1 | Statistical approach for power estimation | 20041125 703/18 |
| US 20040212367 A1 | Battery characterization system | 20041028 324/426 |
| US 20040117172 A1 | Simulation apparatus, method and program | 20040617 703/22 |
| US 20040078182 A1 | Simulation system for multi-node process control systems | 20040422 703/22 |
| US 20040078179 A1 | Logic verification system | 20040422 703/15 |
| US 20040060019 A1 | METHOD AND APPARATUS FOR HIERARCHICAL CLOCK TREE ANALYSIS | 20040325 716/6 |
| US 20040059442 A1 | Systems and methods for designing, simulating and analyzing transportation systems | 20040325 700/30 |
| US 20040054515 A1 | Methods and systems for modeling the performance of a processor | 20040318 703/22 |
| US 20040034837 A1 | Numerically modeling inductive circuit elements | 20040219 716/1 |
| US 20030236656 A1 | Battery characterization system | 20031225 703/14 |
| US 20030225558 A1 | Logic simulation method for information handling system incorporated with memory macro | 20031204 703/15 |
| US 20030217248 A1 | Method and system for instruction-set architecture simulation using just in time compilation | 20031120 712/208 |
| US 20030204819 A1 | Method of generating development environment for developing system LSI and medium which st | 20031030 716/1 |
| US 20030192032 A1 | System and method for debugging a software program | 20031009 717/124 |
| US 20030191869 A1 | C-API instrumentation for HDL models | 20031009 719/328 |
| US 20030191621 A1 | Method and system for reducing storage and transmission requirements for simulation results | 20031009 703/17 |
| US 20030191620 A1 | Dynamic loading of C-API HDL model instrumentation | 20031009 703/17 |
| US 20030191618 A1 | Method and system for reducing storage requirements of simulation data via keyword restriction | 20031009 703/13 |
| US 20030191617 A1 | Method and system for selectively storing and retrieving simulation data utilizing keywords | 20031009 703/13 |
| US 20030188267 A1 | Circuit and method for modeling I/O | 20031002 716/1 |
| US 20030182639 A1 | Circuit simulator system and method | 20030925 716/4 |
| US 20030167454 A1 | Method of and system for providing metacognitive processing for simulating cognitive tasks | 20030904 717/104 |
| US 20030163298 A1 | Reconfigurable measurement system utilizing a programmable hardware element and fixed hard | 20030828 703/21 |
| US 20030156143 A1 | Anesthesia drug monitor | 20030821 345/848 |
| US 20030154061 A1 | Method for semi-automatic generation and behavioral comparison of models | 20030814 703/4 |
| US 20030149962 A1 | Simulation of designs using programmable processors and electronically re-configurable logic ar | 20030807 717/135 |
| US 20030144828 A1 | Hub array system and method | 20030731 703/21 |
| US 20030135354 A1 | Tracking coverage results in a batch simulation farm network | 20030717 703/13 |
| US 20030132973 A1 | System, method and computer program product for intuitive interactive navigation control in virtu | 20030717 345/850 |
| US 20030130831 A1 | Non-unique results in design verification by test programs | 20030710 703/22 |
| US 20030125915 A1 | Count data access in a distributed simulation environment | 20030703 703/13 |
| US 20030105620 A1 | System, method and article of manufacture for interface constructs in a programming language | 20030605 703/22 |
| US 20030101382 A1 | Fail thresholding in a batch simulation farm network | 20030529 714/39 |
| US 20030101041 A1 | Annealing harvest event testcase collection within a batch simulation farm | 20030529 703/22 |
| US 20030101039 A1 | Maintaining data integrity within a distributed simulation environment | 20030529 703/16 |
| US 20030101038 A1 | Centralized disablement of instrumentation events within a batch simulation farm network | 20030529 703/16 |

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| US 20030101035 A1 | Non-redundant collection of harvest events within a batch simulation farm network | 20030529 703/13 |
| US 20030093250 A1 | System, method and computer product for incremental improvement of algorithm performance d | 20030515 703/2 |
| US 20030090491 A1 | Simulation device | 20030515 345/473 |
| US 20030074177 A1 | System, method and article of manufacture for a simulator plug-in for co-simulation purposes | 20030417 703/22 |
| US 20030061580 A1 | Simulation method and compiler for hardware/software programming | 20030327 716/4 |
| US 20030060987 A1 | Systems and methods for estimation and analysis of mechanical property data associated with it | 20030327 702/42 |
| US 20030046671 A1 | System, method and article of manufacture for signal constructs in a programming language cap | 20030306 717/141 |
| US 20030046668 A1 | System, method and article of manufacture for distributing IP cores | 20030306 717/131 |
| US 20030040896 A1 | Method and apparatus for cycle-based computation | 20030227 703/13 |
| US 20030038842 A1 | System and method for configuring a reconfigurable system | 20030227 715/763 |
| US 20030037321 A1 | System, method and article of manufacture for extensions in a programming language capable o | 20030220 717/149 |
| US 20030033594 A1 | System, method and article of manufacture for parameterized expression libraries | 20030213 717/141 |
| US 20030033588 A1 | System, method and article of manufacture for using a library map to create and maintain IP cor | 20030213 717/107 |
| US 20030028864 A1 | System, method and article of manufacture for successive compilations using incomplete param | 20030206 717/141 |
| US 20030023740 A1 | System and method for operating software in a flight simulator environment | 20030130 709/230 |
| US 20030009746 A1 | Variable accuracy modes in microprocessor simulation | 20030109 717/135 |
| US 20020199173 A1 | System, method and article of manufacture for a debugger capable of operating across multiple | 20021226 717/129 |
| US 20020193977 A1 | Method and apparatus for simulating electronic circuits having conductor or dielectric losses | 20021219 703/15 |
| US 20020183997 A1 | Apparatus and method for specifying the configuration of mixed-language simulation models | 20021205 703/13 |
| US 20020170037 A1 | Apparatus and method for controlling event ordering in a mixed- language simulator | 20021114 717/131 |
| US 20020166110 A1 | Apparatus and method for performing event processing in a mixed-language simulator | 20021107 717/106 |
| US 20020152060 A1 | Inter-chip communication system | 20021017 703/17 |
| US 20020150866 A1 | Integrated evaluation and simulation system for ground combat vehicles | 20021017 434/62 |
| US 20020133325 A1 | Discrete event simulator | 20020919 703/17 |
| US 20020073375 A1 | Method and apparatus for test generation during circuit design | 20020613 714/739 |
| US 20020062207 A1 | Computer-implemented system and method for simulating motor vehicle and bicycle traffic | 20020523 703/8 |
| US 20020059054 A1 | Method and system for virtual prototyping | 20020516 703/20 |
| US 20020042703 A1 | Method and system for analyzing behavior of whole human body by simulation using whole hum: | 20020411 703/11 |
| US 20020041248 A1 | Digital cancellation of D/A converter noise in pipelined A/D converters | 20020411 341/156 |
| US 20020035518 A1 | Method and system and computer program product for providing commodity information | 20020321 705/26 |
| US 20020032559 A1 | Hardware and software co-simulation including executing an analyzed user program | 20020314 703/22 |
| US 20020022939 A1 | Control program development support apparatus | 20020221 702/123 |
| US 20020019969 A1 | Hardware and software co-simulation including simulating the cache of a target processor | 20020214 716/5 |
| US 20020016700 A1 | Method and system for analyzing behavior of whole human body by simulation using whole hum: | 20020207 703/6 |
| US 20010036242 A1 | In-core fixed nuclear instrumentation system and power distribution monitoring system | 20011101 376/245 |
| US 7085703 B2 | Count data access in a distributed simulation environment | 20060801 703/17 |
| US 7085670 B2 | Reconfigurable measurement system utilizing a programmable hardware element and fixed hard | 20060801 702/127 |
| US 7058896 B2 | System, method and computer program product for intuitive interactive navigation control in virtu | 20060606 715/757 |
| US 7058562 B2 | Apparatus and method for performing event processing in a mixed-language simulator | 20060606 703/22 |
| US 7050958 B1 | Method and apparatus for accelerating hardware simulation | 20060523 703/15 |
| US 7050950 B2 | System, method and computer product for incremental improvement of algorithm performance d | 20060523 703/2 |
| US 7036114 B2 | Method and apparatus for cycle-based computation | 20060425 717/149 |
| US 7027971 B2 | Centralized disablement of instrumentation events within a batch simulation farm network | 20060411 703/14 |
| US 7024660 B2 | Debugging a program intended to execute on a reconfigurable device using a test feed-through c | 20060404 717/124 |

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| US 7024399 B2 | Computer architecture and process of patient generation, evolution, and simulation for computer | 20060404 706/45 |
| US 7006028 B2 | Digital background cancellation of digital to analog converter mismatch noise in analog to digital | 20060228 341/155 |
| US 6997715 B2 | Integrated evaluation and simulation system for ground combat vehicles | 20060214 434/11 |
| US 6996513 B2 | Method and system for identifying inaccurate models | 20060207 703/14 |
| US 6993469 B1 | Method and apparatus for unified simulation | 20060131 703/15 |
| US 6983227 B1 | Virtual models of complex systems | 20060103 703/2 |
| US 6963827 B1 | System and method for performing discrete simulation of ergonomic movements | 20051108 703/6 |
| US 6961690 B1 | Behavioral digital simulation using hybrid control and data flow representations | 20051101 703/18 |
| US 6961689 B1 | Scheduling non-integral simulation time for mixed-signal simulation | 20051101 703/17 |
| US 6950788 B2 | Computer-implemented system and method for simulating motor vehicle and bicycle traffic | 20050927 703/8 |
| US 6934885 B2 | Fail thresholding in a batch simulation farm network | 20050823 714/33 |
| US 6925431 B1 | Method and system for predicting communication delays of detailed application workloads | 20050802 703/17 |
| US 6915249 B1 | Noise checking method and apparatus | 20050705 703/14 |
| US 6912494 B1 | Method of reducing delays | 20050628 703/4 |
| US 6871298 B1 | Method and apparatus that simulates the execution of parallel instructions in processor function | 20050322 714/33 |
| US 6868454 B1 | Distributed-object development system and computer-readable recording medium recorded with | 20050315 709/237 |
| US 6865526 B1 | Method for core-based system-level power modeling using object-oriented techniques | 20050308 703/18 |
| US 6832182 B1 | Circuit simulator | 20041214 703/13 |
| US 6813598 B1 | Logic simulation method and logic simulation apparatus | 20041102 703/14 |
| US 6810442 B1 | Memory mapping system and method | 20041026 710/22 |
| US 6810373 B1 | Method and apparatus for modeling using a hardware-software co-verification environment | 20041026 703/14 |
| US 6804636 B2 | Control program development support apparatus | 20041012 703/13 |
| US 6785873 B1 | Emulation system with multiple asynchronous clocks | 20040831 716/4 |
| US 6785642 B1 | Method of converting data | 20040831 703/14 |
| US 6754763 B2 | Multi-board connection system for use in electronic design automation | 20040622 710/317 |
| US 6751583 B1 | Hardware and software co-simulation including simulating a target processor using binary transi | 20040615 703/17 |
| US 6734818 B2 | Digital cancellation of D/A converter noise in pipelined A/D converters | 20040511 341/161 |
| US 6711531 B1 | Temperature control simulation method and apparatus | 20040323 703/6 |
| US 6691301 B2 | System, method and article of manufacture for signal constructs in a programming language cap | 20040210 717/114 |
| US 6687889 B1 | Method and apparatus for hierarchical clock tree analysis | 20040203 716/6 |
| US 6651225 B1 | Dynamic evaluation logic system and method | 20031118 716/4 |
| US 6650731 B1 | Simulator for simulating an intelligent network | 20031118 379/15.01 |
| US 6606734 B2 | Simulation method and compiler for hardware/software programming | 20030812 716/4 |
| US 6606721 B1 | Method and apparatus that tracks processor resources in a dynamic pseudo-random test progr | 20030812 714/728 |
| US 6584436 B2 | Hardware and software co-simulation including executing an analyzed user program | 20030624 703/13 |
| US 6530054 B2 | Method and apparatus for test generation during circuit design | 20030304 714/739 |
| US 6493863 B1 | Method of designing semiconductor integrated circuit | 20021210 716/18 |
| US 6427224 B1 | Method for efficient verification of system-on-chip integrated circuit designs including an embed | 20020730 716/4 |
| US 6425762 B1 | System and method for cosimulation of heterogeneous systems | 20020730 434/29 |
| US 6421251 B1 | Array board interconnect system and method | 20020716 361/788 |
| US 6408041 B2 | In-core fixed nuclear instrumentation system and power distribution monitoring system | 20020618 376/254 |
| US 6393379 B1 | Converfication system and method | 20020514 703/14 |
| US 6370494 B1 | Simulator and computer-readable recordable medium having program for execution on computer | 20020409 703/17 |
| US 6347388 B1 | Method and apparatus for test generation during circuit design | 20020212 714/739 |

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| US 6321366 B1 | Timing-insensitive glitch-free logic system and method | 20011120 716/6 |
| US 6321363 B1 | Incremental simulation using previous simulation results and knowledge of changes to simulator | 20011120 716/4 |
| US 6310929 B1 | In-core fixed nuclear instrumentation system and power distribution monitoring system | 20011030 376/245 |
| US 6310619 B1 | Virtual reality, tissue-specific body model having user-variable tissue-specific attributes and a sy | 20011030 345/420 |
| US 6263302 B1 | Hardware and software co-simulation including simulating the cache of a target processor | 20010717 703/17 |
| US 6230114 B1 | Hardware and software co-simulation including executing an analyzed user program | 20010508 703/13 |
| US 6182258 B1 | Method and apparatus for test generation during circuit design | 20010130 714/739 |
| US 6134516 A | Simulation server system and method | 20001017 703/27 |
| US 6110219 A | Model for taking into account gate resistance induced propagation delay | 20000829 716/1 |
| US 6110217 A | System and method for synchronization of multiple analog servers on a simulation backplane | 20000829 703/14 |
| US 6099574 A | Method and apparatus for obtaining structure of semiconductor devices and memory for storing | 20000808 703/14 |
| US 6052524 A | System and method for simulation of integrated hardware and software components | 20000418 703/22 |
| US 6026230 A | Memory simulation system and method | 20000215 703/13 |
| US 5999734 A | Compiler-oriented apparatus for parallel compilation, simulation and execution of computer progr | 19991207 717/149 |
| US 5991533 A | Verification support system | 19991123 703/28 |
| US 5980096 A | Computer-based system, methods and graphical interface for information storage, modeling and | 19991109 707/100 |
| US 5978576 A | Computer performance modeling system and method | 19991102 703/22 |
| US 5978571 A | Method and apparatus for synchronous circuit simulation design by eliminating unneeded timing | 19991102 703/23 |
| US 5963746 A | Fully distributed processing memory element | 19991005 712/20 |
| US 5963731 A | Method of assisting execution of plural simulation programs for coupled simulation | 19990928 703/21 |
| US 5960181 A | Computer performance modeling system and method | 19990831 703/13 |
| US 5946474 A | Simulation of computer-based telecommunications system | 19990803 703/15 |
| US 5933356 A | Method and system for creating and verifying structural logic model of electronic design from bel | 19990622 703/11 |
| US 5914891 A | System and method for simulating operation of biochemical systems | 19990608 703/23 |
| US 5911059 A | Method and apparatus for testing software | 19990420 716/10 |
| US 5896300 A | Methods, apparatus and computer program products for performing post-layout verification of m | 19990105 703/21 |
| US 5857093 A | Cross-compiled simulation timing backannotation | 19981117 703/13 |
| US 5838949 A | System and method for execution-sequenced processing of electronic design simulation results | 19980929 703/18 |
| US 5815416 A | Method of measuring energy consumption in a circuit simulator | 19980526 703/22 |
| US 5758123 A | Verification support system | 19980210 712/20 |
| US 5717943 A | Advanced parallel array processor (APAP) | 19971223 703/17 |
| US 5701439 A | Combined discrete-event and continuous model simulation and analysis tool | 19971014 703/22 |
| US 5678028 A | Hardware-software debugger using simulation speed enhancing techniques including skipping u | 19971014 703/13 |
| US 5677856 A | Simulation apparatus for circuit verification | 19970902 703/4 |
| US 5663890 A | Method, apparatus and computer program product for determining a frequency domain responsi | 19970429 703/21 |
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| US 5553008 A | Transistor-level timing and simulator and power analyzer | 19960813 703/14 |
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| L# | Hits | Search String | Databases |
|-----|-------|--|-----------|
| L1 | 12367 | (microprocessor\$1 or microcomputer\$1 or computer\$1 or (integrated near2 circuit)) with simr | US-PGPUB |
| L2 | 1631 | 1 and ((function\$2 or behavior\$2) near2 simulat\$3) | US-PGPUB |
| L3 | 2084 | 1 and ((performance or ((delay or cycle or execution or access) near2 tim\$3) or (cycle near2 | US-PGPUB |
| L4 | 679 | 2 and 3 | US-PGPUB |
| L5 | 30 | 4 and (accuracy near2 (level or modify\$3 or vary\$3 or alter\$3)) | US-PGPUB |
| L6 | 5 | 5 and (functional.CLM.) | US-PGPUB |
| L7 | 6 | 5 and (performance.CLM.) | US-PGPUB |
| L8 | 8 | 5 and (accuracy.CLM.) | US-PGPUB |
| L9 | 2 | 5 and (behavioral.CLM.) | US-PGPUB |
| L10 | 14 | 6 or 7 or 8 or 9 | US-PGPUB |

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Results of search set S24:

| Document Kind | Codes | Title | Issue Date | Current OR | Abstract |
|---------------|----------------|---|------------|------------|----------|
| US | 20060155411 A1 | Model based testing for electronic devices | 20060713 | 700/108 | |
| US | 20060150132 A1 | Method and system for finding an equivalent circuit representation for one or more elements | 20060706 | 716/5 | |
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| US | 20030060987 A1 | Systems and methods for estimation and analysis of mechanical property data associated w | 20030327 | 702/42 | |
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| US | 20020042703 A1 | Method and system for analyzing behavior of whole human body by simulation using whole l | 20020411 | 703/11 | |
| US | 20020032559 A1 | Hardware and software co-simulation including executing an analyzed user program | 20020314 | 703/22 | |
| US | 20020019969 A1 | Hardware and software co-simulation including simulating the cache of a target processor | 20020214 | 716/5 | |
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